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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,657	05/15/2001	Boon Seong Ang	10004260	1132

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EXAMINER	
TRUONG, CAMQUY	
ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,657	ANG, BOON SEONG	
	Examiner	Art Unit	
	Camquy Truong	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

3. It is noted that although the present application does contain line numbers in the specification and claims, the line numbers in the claims do not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the examiner and Applicant all future correspondence should include the recommended line numbering.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack proper antecedent basis:

(i) The first process – claim 23, line 9;

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-7, 11-16, 18-19 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrell et al (U.S. Patent 5,630,128).

8. As to claims 1 and 22, Farrell teaches the invention substantially as claimed including: A method for thread scheduling to run in parallel with a processor (col.1, lines 30-33; col. 5, lines 11-13; col.11, lines 37-38), comprising the steps of:

Obtaining parameter values for a plurality of different threads (col. 3, lines 51-53; col. 3, line 59 – col.4, line 2);

Performing logic functions (promote primitive function, col. 5, line 17), in parallel with, without interrupting the main processor (col.5, lines 10-13), on said parameter values to determine if thread scheduling should be reconfigured (col.4, lines 35-42), and if so, which thread should be enabled (col.5, lines 15-18, lines 25-28, lines 39-43, lines 50-52, and line 66; col.6 lines 3-5 and lines 25-28);

Sending an interrupt signal to interrupt the main processor if thread scheduling is to be reconfigured (col. 12, lines 3-5 and lines 28-31).

9. Farrell does not explicitly teach that the processor is a main processor. However, Farrell et al teach that their system has different computer processors that run in parallel (14a, 14b and 14c, Fig. 1; col. 1, lines 31-34; col. 3, lines 30-31).

10. It would have been obvious to one of ordinary skill in the art at the time the invention was made that Farrell's system in fact provides the main processor that can run a multitasking operating system which optimizes the execution of threads, while permitting application programs to substantially influence the execution schedule.

11. As to claim 23, it is rejected for the same reason as claim 1. In addition, Farrell teaches logic for triggering a second process to run after the first process to perform second logic functions to determine which thread should be enabled when at least one second parameter is updated during a period when the first process is running (col. 6, lines 23-28 and lines 34-36).

12. As to claim 2, Farrell teaches the step of performing logic functions performed on a continuous basis (col. 3, lines 43-46).

13. As to claim 3, Farrell teaches the obtaining parameter values step comprise monitoring the values from thread processes held in memory mapped

registers with fixed addresses (col.3, lines 40-42; col. 4, lines 43-49; col.6, lines 7-12;col.5, lines 39-43; col.15, lines 39-42).

14. As to claim 4, Farrell teaches performing logic functions step comprise performing said logic functions substantially simultaneously on a substantial plurality of said parameter (col. 3, line 43-49).

15. As to claims 5-6, Farrell teaches performing logic functions step comprise performing logic functions on reconfigurable hardware (col.5, lines 14-52).

16. As to claim 7, during the performing logic functions step, receiving at least one additional parameter value; and performing logic functions with said at least one additional parameter value to determine if thread rescheduling should be reconfigured (col.5, lines 14-16 and lines 25-28; lines 39-43 and lines 50-52).

17. As to claim 11, Farrell teaches local copies of the parameter value are held in a set of registers and wherein said obtaining step comprises snooping memory operations for data addressed to a plurality of predetermined locations and updating the local copies thereof in the set of registers (col.5, lines 51-52; col. 6, lines 5-13).

18. As to claim 12, Farrell teaches snooping memory operations include memory operations for the processors in a multiprocessor system (col.4, lines, 25-28 and 43-49).

19. As to claim 13, Farrell teaches receiving at least one additional parameter value during the performance of the performing logic functions step; and when the initial performance of the performing logic functions steps is completed, performing logic functions with said at least one additional parameter value to determine if thread rescheduling should be reconfigured (col.5, lines 14-16 and lines 25-28; lines 39-43 and lines 50-52).

20. As to claim 14, Farrell teaches parameter values is a time devoted to a currently running thread (col.3, lines 40-41; col. 4 lines 1-2).

21. As to claim 15, Farrell teaches one of said parameter values is an amount of data that a predetermined queue is able to produce (col.5, line26-28).

22. As to claim 16, Farrell teaches one of the parameter values is an amount of data that may be consumed by a predetermined queue (col. 5, lines 42-49).

23. As to claim 18, Farrell teaches the performing logic function step comprises storing interim and or final results from the performing logic step (col. 5, lines 51-52; col. 6, lines 7-10).

24. As to claim 19, Farrell teaches the performing logic functions step includes the step of determining when a parameter value for a thread has been modified and determining an identity of the parameter that has been modified; and, wherein said performing logic functions step is performed with said identity of the modified parameter used, in part, to pick a specific logic function to perform (col. 5, lines 21-28, lines 39-49).

25. Claims 8-10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrell et al. (U.S. Patent 5,630,128) as applied to claim 1 above, in the view of Borkenhagen et al (U.S. Patent 6,567,839 B1).

26. As to claim 8, Farrell does not explicitly teach the performing logic functions step comprise performing said logic functions with a microengine or microprocessor. However, Borkenhagen teaches microprocessor (col.2, line 62).

27. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Farrell and Borkenhagen

because Borkenhagen's microprocessor would improve in overall speed of the computer system by reduced instruction set computer (RISC) architecture characterized by a small simplified set of frequently used instructions for rapid execution and perform quicker.

28. As to claim 9, Farrell teaches during performing logic functions step in the microengine, receiving at least one additional parameter value; and when the microengine or microprocessor is free, performing logic functions with said at least one additional parameter value to determine if thread rescheduling should be reconfigured (col. 4, lines 54-57; col.5, lines 14-16, lines 25-28, lines 39-43 and lines 50-52).

29. As to claim 10, Farrell teaches the perform logic functions with the at least one additional parameter comprises performing a different logic function as compared to an immediately preceding logic function performed in the performing logic functions step (col.5, lines 42-50)

30. As to claim 17, Borkenhagen teaches the thread scheduling function and the function of the main processor are performed on a single chip (col. 2, lines 61-62).

31. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrell et al. (U.S. Patent 5,630,128), as applied to claim 1 above, in view of Belo (U.S. Patent 5,379,428).

32. As to claim 20, Farrell teaches the invention substantially as claimed including: a parallel hardware thread scheduler (col.1, lines 30-33; col. 5, lines 11-13; col.11, lines 37-38), comprising:

A main processor (col. 3, lines 30-31);

A plurality of memory mapped registers (thread state descriptor, col. 4, line 26), each of said registers holding a different thread parameter (col. 4, lines 25-28 and 43-49);

Reconfigurable logic (promote primitive function, col. 5, line17) connected to received a substantial plurality of outputs from said registers (col. 5, lines 15-17) in parallel (col. 5, lines 10-13) and to perform logic functions substantially simultaneously thereon (col. 3, lines 47-49; col. 4, lines 25-28 and lines 43-49), in parallel with, without interrupting the main processor, to determine if thread scheduling should be reconfigured (col.4, lines 35-42), and if so, determining which thread should be enabled (col.5, lines 15-18, lines 25-28, lines 39-43, lines 50-52, and line 66; col.6 lines 3-5 and lines 25-28);

A circuit for sending an interrupt signal to interrupt the processor if thread scheduling is to be reconfigured (col. 12, lines 26-31).

33. Farrell does not explicitly teach the hardware logic. However, Belo teaches the hardware logic for process scheduler (Fig. 3; col. 3, lines 29 -30).

34. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Farrell and Belo because Belo 's hardware logic would improve the decision speed by eliminating the use of scheduling software and dispatching processes to hardware logic for quick and efficient processes.

35. As to claim 21, it is rejected for the same reason as claim 20. In addition, Farrell teaches a snooping detecting from memory traffic selected addresses for parameter values for a plurality of different threads (col. 4, lines 43-49), including a set of register for holding local copies of said parameter values with said selected addresses (col. 6, lines 7-10), and logic for updating one of said local copies when the address therefor has been detected (col. 5, lines 39-52; col. 6, lines 7-10).

Conclusion

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Camquy Truong whose telephone number is (703) 305 - 8888. The examiner can normally be reached on 8 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 703-305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

Camquy Truong

August 6, 2004

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